translated version thereof). Other aspects of the invention include test circuitry for use in a circuit having an access node and methods for performing on-chip testing, configuration, and control of operational circuitry within a chip in response to test data and at least one control signal asserted from an external source to an external node.

IN THE CLAIMS:

Amend claims 1 and 28 to read as follows [attached is an appendix including a marked up version of the amended claim showing the difference between the claim as originally filed, and the claim as hereby amended]:

1. (Amended) An integrated circuit, comprising:

an external node;

operational circuitry; and

test circuitry coupled to the external node and the operational circuitry, wherein the test circuitry is configured to operate in at least one test mode in response to test data received at the external node from an external source, and the test circuitry is configured to assert to the operational circuitry a control signal in response to an external control signal received at the external node.

28. (Amended) A method for controlling operational circuitry within an integrated circuit, and performing at least one of testing, configuration, and reconfiguration of the operational circuitry, wherein the integrated circuit has an external node and the operational circuitry is configured to operate in response to at least one control signal, said method including the steps of:

operating test circuitry of the integrated circuit in at least one test mode in response to test data received at the external node from an external source; and

asserting said at least one control signal from the test circuitry to the operational circuitry in response to an external control signal received at the external node.

Add the following new claims:

41. (New) The integrated circuit of claim 1, wherein the operational circuitry is configured to operate in response to the control signal.

42. (New) The integrated circuit of claim 41, said integrated circuit also including at least one additional external node.

43. (New) The integrated circuit of claim 1, wherein the operational circuitry is configured to operate in response to the control signal and at least one additional control signal.

44. (New) The integrated circuit of claim 43, said integrated circuit also including at least one additional external node.

REMARKS:

Claims 1-20 stand rejected under 35 U.S.C. 112, second paragraph, as being indefinite. In response, claim 1 is amended to eliminate any possible ambiguity as to the antecedent basis for the expression "the external node" and the relation between the recited "control signal" and other claim elements. New claims 41-44 are added to claim subsets of the subject matter of claim 1. Claim 41 recites that the operational circuitry of claim 1 is configured to operate in response to the control signal of claim 1. Claim 43 recites that the operational circuitry of claim 1 is configured to operate in response to the control signal of claim 1 and at least one additional control signal. Claims 42 and 44 recite that the integrated circuit includes at least one additional external node (in addition to the external node recited in claim 1).

Claims 1 and 28 stand rejected under 35 U.S.C. 102(e) as being anticipated by U.S. Patent Application Publication No. 2002/0097616 ("Schneider"). In response, Claim 28 is amended to correct to minor grammatical and typographical errors, and Applicants contend

that Schneider is not properly cited as prior art and that claims 1 and 28 as hereby amended are patentable over the other references of record.

In view of the attached Declaration under 37 CFR 1.131 by the inventors, the attached declaration by Paul Werking in support of the Declaration under 37 CFR 1.131, and the attachments to these two declarations, Applicants respectfully contend that they have established an invention date prior to the effective date of Schneider (January 23, 2002) for the invention of claims 1 and 28. As established by attached declarations (and the attachments to the declarations), the invention of claims 1 and 28 was conceived in the U.S. prior to January 23, 2002 (the "Critical Date") and inventor Kyle Fodchuk worked diligently and reasonably continuously in the U.S. during the period from January 14, 2002, through February 4, 2002, toward reducing to practice the invention of claims 1 and 28.

Claims 1 and 28 as amended (and new claims 41-44) have not been rejected over, and are believed to be patentable over, the references of record other than Schneider.

Claims 2-6, 9, 21-24, and 29-32 stand rejected under 35 U.S.C. 103(a) as being unpatentable over Schneider in view of U.S. Patent 6,289,055 ("Knotz"). In response, Applicants contend (for the reasons set forth above) that Schneider is not properly cited as prior art and that claims 2-6, 9, 21-24, and 29-32 are patentable over Knotz for the following reasons.

Knotz fails to disclose an integrated circuit comprising an external node, operational circuitry, and test circuitry coupled to the external node and the operational circuitry (as recited in amended claim 1), test circuitry (for use in a circuit comprising an access node and operational circuitry) comprising logic circuitry configured to be coupled to the access node and to the operational circuitry, and additional circuitry coupled to the logic circuitry and configured to operate in at least one test mode in response to test data received at the access node (as recited in claim 21), or a method (for controlling operational circuitry within an integrated circuit and performing at least one of testing, configuration, and reconfiguration of

the operational circuitry) including the steps of operating test circuitry of the integrated circuit in at least one test mode in response to test data received at an external node, and asserting at least one control signal from the test circuitry to the operational circuitry in response to an external control signal received at the external node (as recited in claim 28). Thus, claim 21, and all claims that depend directly or indirectly from claim 1, 21, or 28, are patentable over Knotz.

Claims 14, 15, and 35 stand rejected under 35 U.S.C. 103(a) as being unpatentable over Schneider in view of U.S. Patent 5,557,571 ("Kato"). In response, Applicants contend (for the reasons set forth above) that Schneider is not properly cited as prior art and that claims 14, 15, and 35 are patentable over Kato for the following reasons.

Kato fails to disclose an integrated circuit comprising an external node, operational circuitry, and test circuitry coupled to the external node and the operational circuitry, wherein the test circuitry is configured to operate in at least one test mode in response to test data received at the external node from an external source, and the test circuitry is configured to assert to the operational circuitry a control signal in response to an external control signal received at the external node (as recited in claim 1) or a method (for controlling operational circuitry within an integrated circuit and performing at least one of testing, configuration, and reconfiguration of the operational circuitry) including the steps of operating test circuitry of the integrated circuit in at least one test mode in response to test data received at an external node, and asserting at least one control signal from the test circuitry to the operational circuitry in response to an external control signal received at the external node (as recited in claim 28). Thus, all claims that depend directly or indirectly from claim 1 or 28 are patentable over Kato.

The Examiner indicates that claims 7, 8, 10-13, and 16-20 would be allowable if rewritten to overcome the rejection under 35 U.S.C. 112, second paragraph, and to include all of the limitations of the base claim and any intervening claims. Applicants respectfully contend that these claims (and the claims from which they depend) are allowable in view of

the attached declarations, the amendments set forth herein, and the discussion herein of the declarations and amendments.

Claims 25-27, 33, 34, and 36-40 have been objected to, but are said to be allowable if rewritten to include all of the limitations of the base claim and any intervening claims. Applicants respectfully contend that these claims (and the claims from which they depend) are allowable in view of the attached declarations, the amendments set forth herein, and the discussion herein of the declarations and amendments.

The Examiner has objected to the abstract. In response, the abstract is hereby amended. Applicants observe that sample abstracts in the cited section of the MPEP (MPEP Section 608.01(b)) include initial phrases that are not complete sentences, and respectfully request that the Examiner identify a basis for any continued requirement that the first phrase of the abstract be replaced by a complete sentence.

Respectfully submitted,

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APPENDIX

Claims 1 and 28 are hereby amended to read as follows:

1. (Amended) An integrated circuit, comprising:

[at least one] an external node;

operational circuitry [configured to operate in response to at least one control signal]; and

test circuitry coupled to the external node and the operational circuitry, wherein the test circuitry is configured to operate in at least one test mode in response to test data received at the external node from an external source, and the test circuitry is configured to assert to the operational circuitry a control signal in response to an external control signal received at the external node.

28. (Amended) A method for controlling operational circuitry within an integrated circuit, and performing at least one of testing, configuration, and reconfiguration [,] of the operational circuitry [within an integrated circuitry], wherein the integrated [circuitry] circuit has an external node and the operational circuitry is configured to operate in response to at least one control signal, said method including the steps of:

operating test circuitry of the integrated circuit in at least one test mode in response to test data received at the external node from an external source; and

asserting said at least one control signal from the test circuitry to the operational circuitry in response to an external control signal received at the external node.

The abstract is hereby amended to read as follows:

An integrated circuit including operational circuitry operable in response to at least one control signal [(e.g., an enable signal)] asserted to an external node from an external source, and test circuitry coupled to the external node and the operational circuitry. In response to data [(preferably including a digital key)] asserted to the external node from an

external source, the test circuitry enters a test mode in which it tests, configures, or reconfigures the operational circuitry. The test circuitry also asserts to the operational circuitry each control signal received at the external node (or an amplified or translated version thereof). [Preferably, the test circuitry can assert test data from within the chip to the external node for transmission to external circuitry, the test circuitry includes logic circuitry coupled to the external node for receiving an input signal from an external source, and the logic circuitry can extract the test data (and preferably also a clock) from the input signal.] Other aspects of the invention include test circuitry for use in a circuit having an access node and methods for performing on-chip testing, configuration, and control of operational circuitry within a chip in response to test data and at least one control signal asserted from an external source to an external node. [Preferably, the test circuitry includes safety features for preventing accidental test mode operation in response to an input signal at the external node, such as circuitry that disables test mode operation unless test data are asserted to the external node with at least a minimum frequency, and lock circuitry that triggers test mode operation only in response to a valid digital key. Preferably, the test circuitry is configured to extract test data, a clock, and a latch signal from an amplitude-modulated input signal at the external node. Preferably, when the test circuitry is neither in the test mode nor a state in which it analyzes test data to identify a digital key, the test circuitry automatically enters a state of reduced power consumption.]